

**Faculty of Engineering and Technology**

**Department of Electrical and Computer Engineering Digital System**

**ENCS 234**

**Verilog project**

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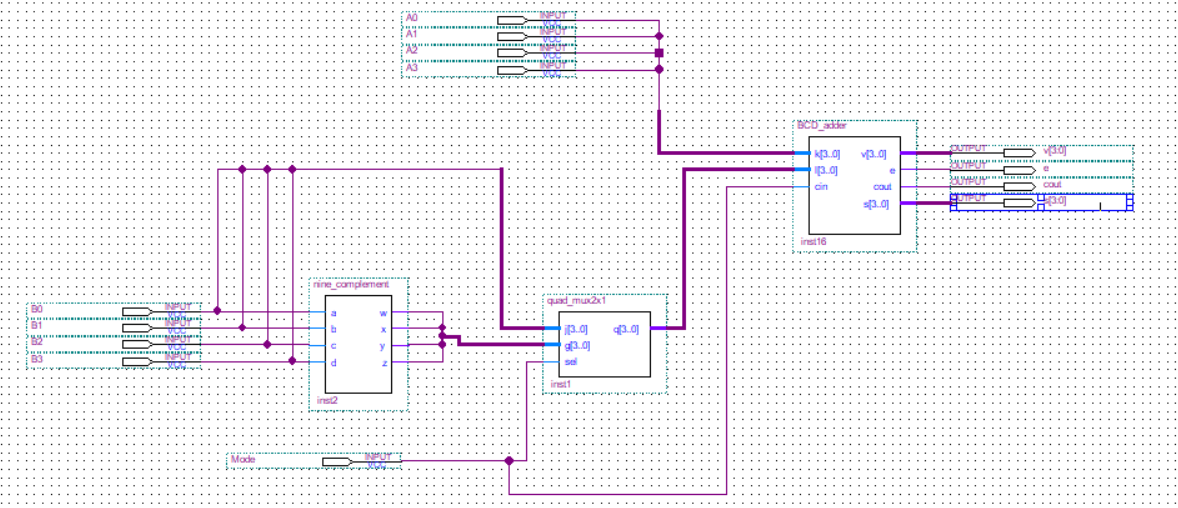
**Student’s Name: Maha Mali**

**ID: #1200746**

**Section: #2**

**Instructor: Dr.Mohammed Hussein**

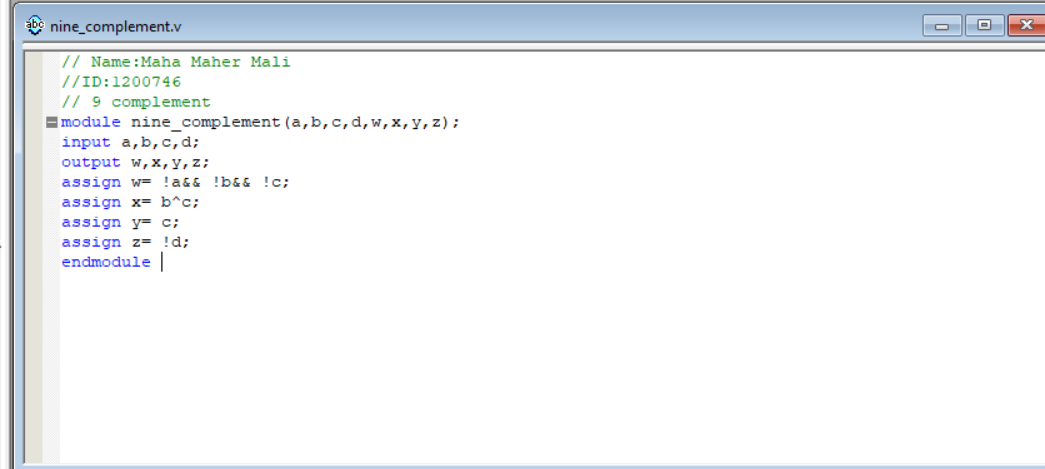
Whole System Design



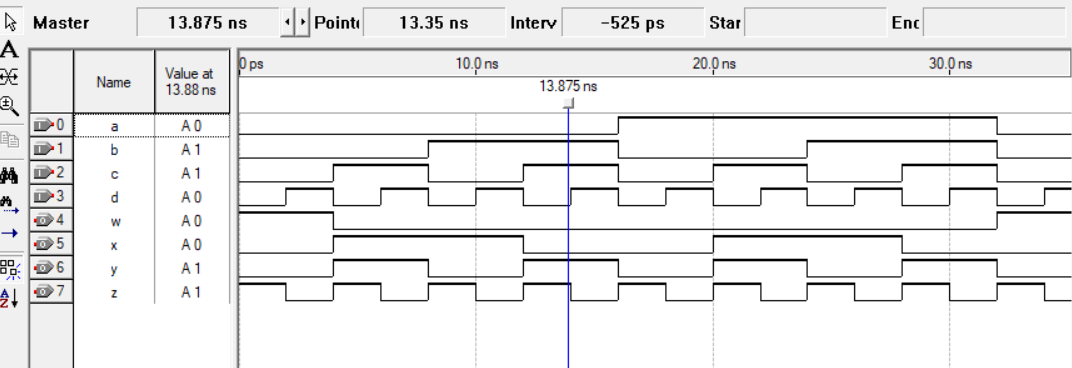
**Part A**

Design a combinational circuit that generates the 9’s complement of a BCD digit. Develop and simulate a **data flow model.**

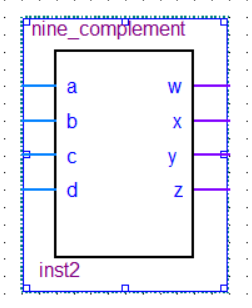
**Code:**

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**Simulation:**

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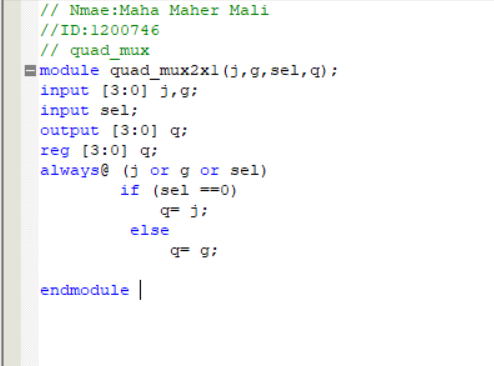
**Block Diagram**

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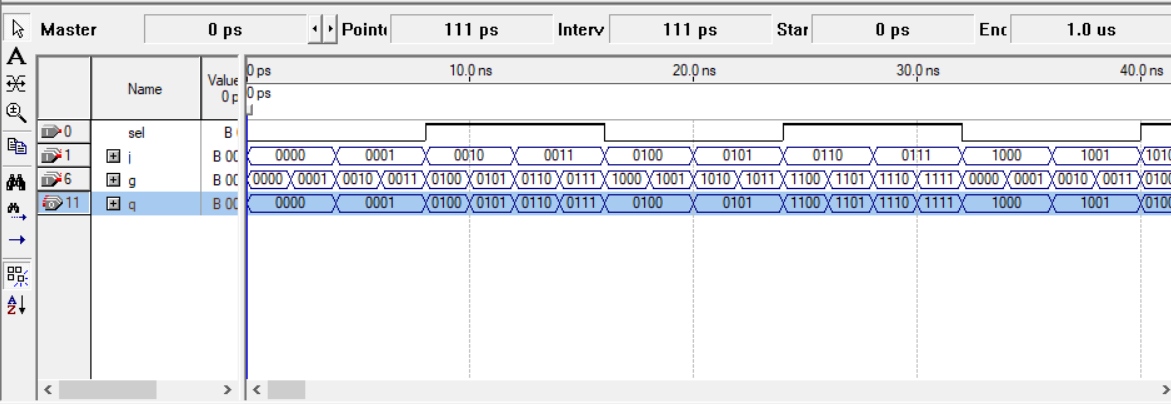
**Part B**

Design a combinational circuit that describes the quadruple 2X1 multiplexer using a **behavioral model.**

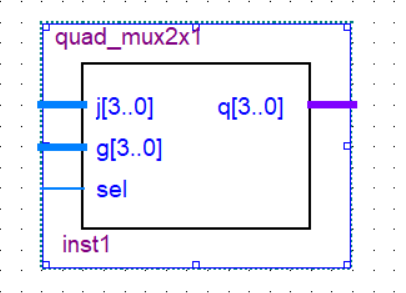
**code**

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**Simulation:**

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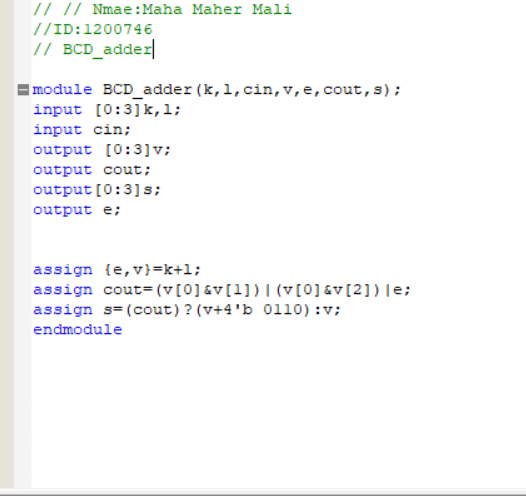
**Block Diagram**

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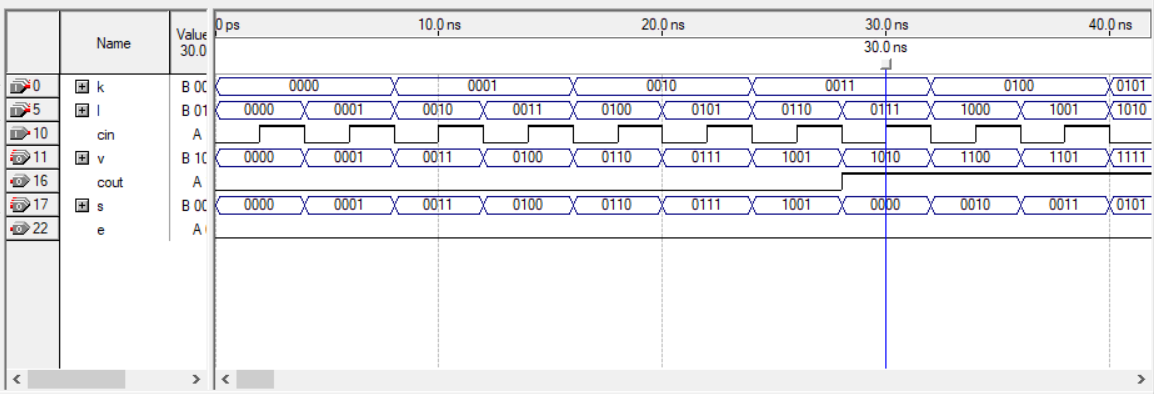
**Part c**

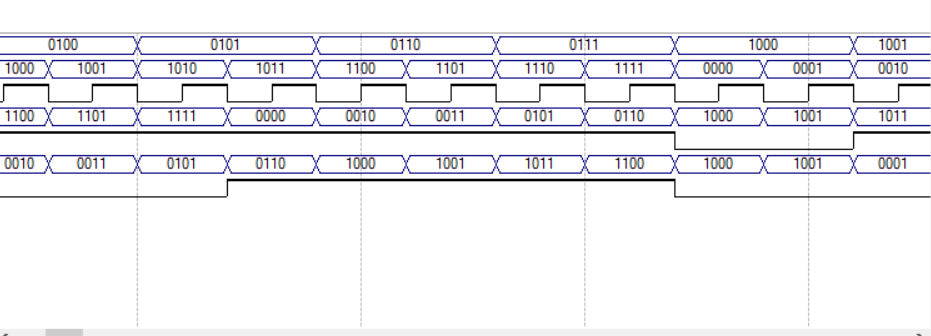
Design a combinational circuit for BCD adder in **data flow model.**

**code**

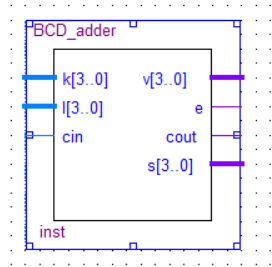
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**Simulation:**

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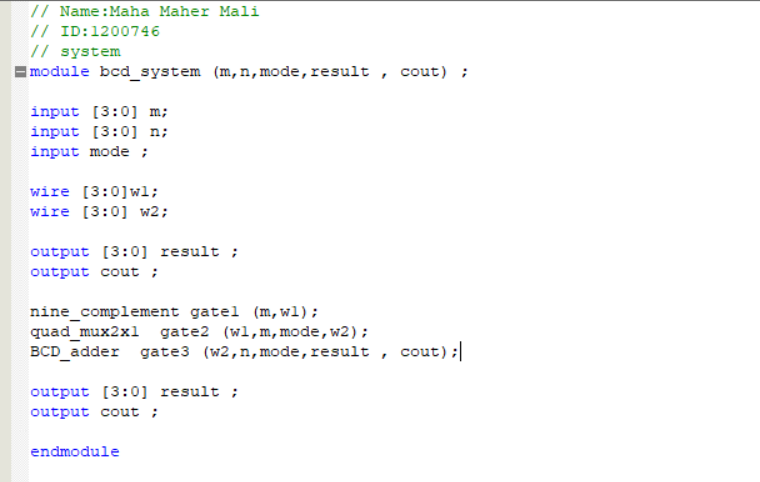
**Block Diagram**

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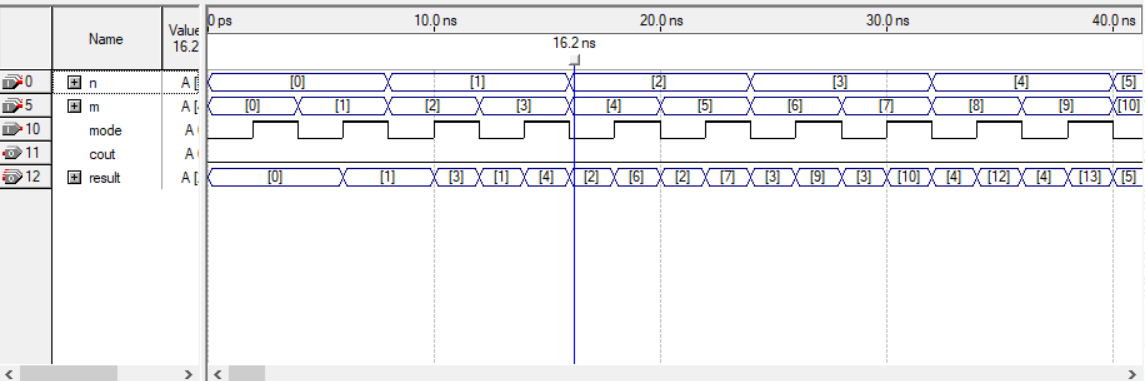
**Part D**

All the system components are to be instantiated in a top-level module using a **structural model.**

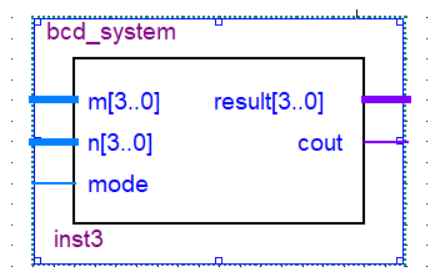
**code**

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**Simulation:**

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**Block Diagram**

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